Notice of Allowability	Application No.	Applicant(s)	
	10/614,341	FLOMAN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 08/15/2005*.

2. ☒ The allowed claim(s) is/are *1,3-12,14-18,20-24 and 27-33*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claims 1-33 are pending in this application. Claims 1, 5, 6, 12-19, 24-26 and 33 have been amended. Claim 2 is cancelled.

2. With the Examiner's Amendment below the claims 1, 4, 6, 12, 14, 16-18, 20-26 and 33 have been amended. Claims 13, 19, 25 and 26 are cancelled. Claims 1, 3-12, 14-18, 20-24 and 27-33 remain in the application.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kenneth Q. Lao on 10/21/2005.

The application has been amended as follows:

Please cancel claims 2, 13, 19, 25 and 26.

Please replace ALL existing claims with the following amended claims.

1. (currently amended) A method for checking a data bus between a first electronic module and a second electronic module operatively connected to the first electronic module, said method comprising:

conveying from the first electronic module to the second electronic module a first bit pattern through the data bus;

receiving in the first electronic module a second bit pattern from the second electronic module through the data bus; the second bit pattern contains at least a part of a ~~reversed~~ complementary pattern of the first bit pattern;

comparing the received second bit pattern to the first bit pattern for determining a usable bus ~~with~~ width of the data bus based on a relationship between the first bit pattern and the ~~reversed~~ complementary pattern of the first bit pattern.

2. (canceled)

3. (original) The method of claim 1, wherein the first bit pattern has an alternate pattern of '0' and '1'.

4. (currently amended) The method of claim 1, wherein each bit in the received first bit pattern and the second bit pattern has a value of either '0' or '1', and second bit pattern is ~~complement~~ complementary to the received first bit pattern such that a bit in the second bit pattern has a value different from the value of the corresponding bit in the received first bit pattern.

5. (currently amended) The method of claim 1, wherein the first electronic module has a maximum bus width defined by a predetermined number of bits and the received second bit pattern has a section in which the pattern is ~~complement~~ complementary to the corresponding part of the first bit pattern, said section having a further number of bits smaller than the predetermined number of bits, and wherein said comparing step determines the usable width of the data bus based on the section in the received second bit pattern.

6. (currently amended) The method of claim 1, further comprising:

conveying to the second electronic module a third bit pattern through the data bus, wherein the third bit pattern contains at least a part of a ~~reverse~~ complementary pattern of the first bit pattern; and

receiving from the second electronic module a fourth bit pattern through the data bus, the fourth bit pattern having the predetermined relationship to the third bit pattern as received in the second electronic module.

7. (original) The method of claim 6, further comprising

comparing the fourth bit pattern as received in the first electronic module to the third bit pattern for determining the usable bus width.

8. (original) The method of claim 1, wherein the second electronic module comprises a memory card.

9. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is equal to the number of bits conveyable on the maximum bus width.

10. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is smaller than the number of bits conveyable on the maximum bus width.

11. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is greater than the number of bits conveyable on the maximum bus width.

12. (currently amended) A software application product embedded in a computer readable medium for use in a first electronic module for checking a data bus between the first electronic module and a second electronic module, said computer readable medium having a plurality of executable codes comprising:

a code for comparing

a first bit pattern provided to the second electronic module through the data bus to

a second bit pattern received through the data bus from the second electronic module, wherein the second bit pattern is provided in response to the first bit pattern as received in the second electronic module, the second bit pattern having at least a part of a ~~reverse~~ complementary pattern of the received first bit pattern; and

a further code for determining a usable bus width of the data bus based on a relationship between the first bit pattern and the complementary pattern of the first bit pattern.

13. (canceled) ~~The software application product of claim 12, the executable codes further comprising~~

~~a further code, based on the predetermined relationship, for determining a usable bus width of the data bus for conveying data between the first electronic module and the second electronic module~~.

14. (currently amended) The software application product of claim 12, wherein the received first bit pattern has an alternate pattern of '0' and '1' and the second bit pattern is ~~complement~~ complementary to the received first bit pattern.

15. (previously presented) The software application product of claim 12, further comprising a third code for generating the first bit pattern.

16. (currently amended) The software application product of claim [[13]] 12, wherein the first electronic module has a maximum bus width defined by a predetermined number of bits, and the received second bit pattern has a section in which the pattern is ~~complement~~ complementary to the corresponding part of the first bit pattern, said section having a further number of bits smaller than the

predetermined number of bits, and wherein the further code determines the usable width of the data bus based on the section in the received second bit pattern.

17. (currently amended) The software application product of claim [[13]] 12, wherein the code also compares

a third bit pattern provided to the second electronic module through the data bus to

a fourth bit pattern received through the data bus from the second electronic module, wherein the third bit pattern is complementary to the first bit pattern and the fourth bit pattern is provided in response to the third bit pattern as received in the second electronic module, and the fourth bit pattern having the predetermined relationship to the received third bit pattern, so as to allow the further code to determine the usable bus width of the data bus.

18. (currently amended) A memory unit for use in an electronic device, the electronic device having a host electronic module for processing data and a data bus for operatively connecting the host module to the memory unit, said memory unit comprising:

means for receiving a first bit pattern from the host module through the data bus; and

means, responsive to the received first bit pattern, for providing a second bit pattern on the data bus, wherein the second bit pattern has at least a part of a ~~reverse~~ complementary pattern of the received first bit pattern, wherein the host electronic module is adapted to compare the first bit pattern to the second bit pattern as received in the host module for determining a usable bus width of the data bus based on a predetermined relationship between the first bit pattern and the complementary pattern of the first bit pattern.

19. (canceled) ~~The memory unit of claim 18, wherein the host electronic module is adapted to compare the first bit pattern to the second bit pattern as received in the host module for determining a usable bus width of the data bus based on a complementary the predetermined relationship between the first bit pattern and the reversed pattern of the first bit pattern.~~

20. (currently amended) The memory unit of claim 18, wherein the received first bit pattern has an alternate pattern of '0' and '1' and the second bit pattern is ~~complement~~ complementary to the received first bit pattern.

21. (currently amended) The memory unit of claim [[19]] 18, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and wherein the number of data pins is smaller than number of data bits conveyable in the maximum bus width.

22. (currently amended) The memory unit of claim [[19]] 18, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and wherein the number of data pins is equal to number of data bits conveyable in the maximum bus width.

23. (currently amended) The memory unit of claim [[19]] 18, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and wherein the number of data pins is greater than number of data bits conveyable in the maximum bus width.

24. (currently amended) An electronic device having means to receive a memory unit, comprising:

a data processing unit;

a data bus linking the data processing unit to the memory unit; and

a program for checking electronic functionality of the data bus, the program comprising:

a code for providing a first bit pattern to the memory unit through the data bus, ~~and~~

a code for requesting the memory unit to provide a second bit pattern, the second bit pattern containing at least a part of a ~~reverse~~ complementary pattern of the first bit pattern,

a code for comparing the first bit pattern with a second bit pattern as received through the data bus from the memory unit, and

a code for determining a usable width of the data bus based on the received second bit pattern based on a complementary relationship between the first bit pattern and the complementary pattern.

25. (canceled) ~~The electronic device of claim 24, wherein the program further comprises~~

~~a further code for comparing the first bit pattern with a second bit pattern as received through the data bus from the memory unit.~~

26. (canceled) ~~The electronic device of claim 25, wherein the program further comprises:~~

~~a third code for determining a usable width of the data bus based on the received second bit pattern based on a complementary relationship between the first bit pattern and the reversed pattern~~.

27. (original) The electronic device of claim 24, wherein said program for checking the electronic functionality of the data bus is carried out at a boot up procedure.

28. (original) The electronic device of claim 24, comprising a mobile phone.

29. (original) The electronic device of claim 24, wherein said memory unit is disposed in a further electronic device.

30. (original) The electronic device of claim 24, wherein the memory unit comprises:

means for receiving the first bit pattern from the data process unit through the data bus; and

means, responsive to the first bit pattern as received through the data bus, for providing the second bit pattern on the data bus.

31. (original) The electronic device of claim 24, wherein the first bit pattern has an alternate pattern of '0' and '1'.

32. (original) The electronic device of claim 24, wherein each bit of the received first bit pattern and the second bit patterns has a value of either '0' or '1', and the second bit pattern is complement to the received first bit pattern.

33. (currently amended) The electronic device of claim [[26]] 24, wherein the program further comprises

a further code for providing a third bit pattern to the memory unit through the data bus, wherein the third bit pattern is complement to the first bit pattern, so as to allow the further code to compare the third bit pattern with a fourth bit pattern received through the data bus from the memory unit, the fourth bit pattern is provided in response to the third bit pattern as received in the memory unit and the fourth bit pattern has the predetermined relationship to the received third bit pattern, and wherein the third code determines the usable width of the data bus also based on the received fourth bit pattern.

Allowable Subject Matter

Claims 1, 3-12, 14-18, 20-24 and 27-33 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to an electronic memory card and its use in a host device and, more particularly, to a method of checking the electrical functionality as related to the usable width of a data bus linking such memory card and host device.

The claimed invention as set forth in claim 1 (broadest claim) recites features such as: a method for checking a data bus between a first electronic module and a second electronic module operatively connected to the first electronic module, which comprises, conveying from the first electronic module to the second electronic module a first bit pattern through the data bus, receiving in the first electronic module a second bit pattern from the second electronic module through the data bus, the second bit pattern contains at least a part of a complementary pattern of the first bit pattern, comparing the received second bit pattern to the first bit pattern for determining a usable bus width of the data bus based on a relationship between the first bit pattern and the complementary pattern of the first bit pattern. In other words, the method for checking the usable width of a data bus linking a host device and a memory card is preferably performed at the boot up process by the host device sending a test bit pattern (first bit pattern) to the memory card through the data bus. Upon receiving the test bit pattern (first bit pattern), the memory card sends a response bit pattern to the host device through the same data bus. The response bit pattern (the second bit pattern) is complement to the test bit pattern so as to allow the host device to compare the response bit pattern with the test bit pattern, and determines the usable width of the data bus based on the comparison result.

The prior arts of record teach a host 51" (first electronic module) connected to multiple memory card sockets 104, 106, and 108 over more than one data line (data bus). Sockets 104, 106, and 108 contain Security Digital (SD) memory cards (second electronic module) which have an increased number of data contacts (data bus). The

host determines the data bus width of the SD card by reading (host's read command is first bit pattern) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). The prior arts of record also teach that the data identifying the data bus width is read from the SCR is stored by the host in a table form (receiving in the first electronic module the second bit pattern from the second electronic module); Cedar et al. (WO-02/15020), and Coyle et al. (US-6473871) are examples of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, upon receiving the test bit pattern, the memory card sends a response bit pattern to the host device through the same data bus. The response bit pattern is complementary to the test bit pattern so as to allow the host device to compare the response bit pattern with the test bit pattern, and determines the usable width of the data bus based on the comparison result. As such, modification of the prior art of record to include the claimed *method for checking the usable width of a data bus linking a host device and a memory card* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *method for checking the usable width of a data bus linking a host device and a memory card* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *method for checking the usable width of a data bus linking a host device and a memory card* as set forth in claim 1. Also, independent claims 12, 18 and 24 have the same limitations as claim 1 which are not anticipated nor rendered obvious

by the prior arts of record. Hence, claims 1, 3-12, 14-18, 20-24 and 27-33 are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefor, the Examiner favors the allowance of claims 1, 3-12, 14-18, 20-24 and 27-33. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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